I. AMENDMENT

in the Claims:

Pl as amend claims 1, 3, 5-8, 13, 17, and 20-23 as follows:

(currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block

having a respective boundary that surrounds the block;

a region disposed outside of the boundaries of between the functional circuit.

- a region disposed <u>outside of the boundaries of between-the</u> functional-circuit blocks and devoid of functional-circuit blocks; and
- a transistor disposed in the region.
- 2. (previously amended) The integrated circuit of claim 1 wherein one of the functional-circuit blocks is configured to perform a predetermined function.
 - (currently amended) An integrated circuit, comprising: functional-circuit blocks that are spaced apart from one another; a region disposed between the functional-circuit blocks and devoid of functional-circuit blocks;
 - a transistor disposed in the region; and

The integrated circuit of claim-1 wherein one of the functional-circuit blocks is unconfigured.

- 4. (original) The integrated circuit of claim 1 wherein the transistor comprises an FET transistor.
 - 5. (currently amended) An integrated circuit, comprising:
 functional-circuit blocks that are spaced apart from one another;
 a region disposed between the functional-circuit blocks and devoid of functional-circuit blocks;
 - a transistor disposed in the region: and

The integrated-circuit of claim 1 wherein the transistor is automatically placed in the devoid region after the functional-circuit blocks are placed.

2

FAX RECEIVED

JUL 2 4 2003

(currently amended) An integrated circuit, comprising:
 functional-circuit blocks that are spaced apart from one another;
 a region disposed between the functional-circuit blocks and devoid of
 functional-circuit blocks;

a transistor disposed in the region; and

The integrated circuit of claim-1-wherein the transistor is manually placed in the devoid region after the functional-circuit blocks are placed.

7. (currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block having a respective boundary that surrounds the block;

- a region located between and outside the boundaries of the functional-circuit blocks and devoid of functional-circuit blocks; and
- a buffer disposed in the region and coupled to one of the functional-circuit blocks.
- 8. (currently amended) An integrated circuit, comprising:

functional-circuit blocks that are spaced apart from one another, each block having a respective boundary that surrounds the block;

- a region located between and outside the boundaries of the functional-circuit blocks and devoid of functional-circuit blocks; and
- a logic circuit disposed in the region and coupled to one of the functional-circuit blocks.
- (original) The Integrated circuit of claim 8 wherein the logic circuit comprises a logic gate.
- 10. (original) The integrated circuit of claim 8 wherein the logic circuit comprises an inverter.
- 11. (allowed) An integrated circuit, comprising:

first and second supply nodes;

functional-circuit blocks that are spaced apart from one another, one of the functional-circuit blocks coupled to the first and second supply nodes;



- a region located between the functional-circuit blocks and devoid of functional-circuit blocks; and
- a translator disposed in the region and having a pair of input-output terminals coupled to the first supply node and having a control terminal coupled terminal coupled terminal supply node.
- 12. (allowed) The integrated circuit of claim 11 wherein:

the transistor comprises an FET transistor;

the pair of input-output terminals comprises a pair of source-drain terminals; and

the control terminal comprises a gate terminal.

- 13. (currently amended) An integrated circuit, comprising:
- a conductive path;
- functional-circuit blocks that are spaced apart from one another, <u>each of the</u>
 <u>blocks having a respective boundary that surrounds the block</u>, one of
 the functional-circuit blocks coupled to the conductive path;
- a region located between and outside the boundaries of the functional-circuit blocks and devoid of functional-circuit blocks; and
- a transistor disposed in the region and having a pair of input-output terminals coupled to the conductive path and having a control terminal.
- 14. (original) The integrated circuit of claim 13, further comprising: a supply node; and wherein the control terminal is coupled to the supply node.
- 15. (original) The integrated circuit of claim 13 wherein the control terminal is coupled to one of the input-output terminals.
- 16. (original) The integrated circuit of claim 13 wherein the control terminal is short-circuited to one of the input-output terminals.

17. (currently amended) An int grated circuit, comprising:

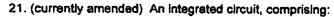
first and second regions that are spaced apart from on another and that have first and second boundaries that respectively surround the first and second and second regions;

- first and second functional-circuit blocks respectively disposed in the first and second regions and entirely within the first and second boundaries;
- a third region located between the first and second functional-circuit blocks and outside of the first and second boundaries and devoid of functional-circuit blocks;
- a buffer disposed in the third region and having an input terminal and an output terminal;
- a first conductive path having a first terminal coupled to the first functional-circuit block and having a second terminal coupled to the input terminal of the buffer, and
- a second conductive path having a first terminal coupled to the output terminal of the buffer and having a second terminal coupled to the second functional-circuit block.
- 18. (previously amended) The integrated circuit of claim 17 wherein the first and second functional-circuit blocks are operable to perform first and second predetermined functions, respectively.
- 19. (previously amended) The integrated circuit of claim 17, further comprising:
- a supply node; and
- wherein the buffer comprises a transistor disposed in the third region and having a control terminal coupled to the input terminal of the buffer, a first terminal coupled to the output terminal of the buffer, and a second terminal coupled to the supply node.
- 20. (currently amended) An integrated circuit, comprising:

first and second regions that are spaced apart from one another and that have first and second boundaries that respectively surround the first and second and second regions:



- first and second functional-circuit blocks that are respectivily disposed in the first and second regions and entirely within the first and second boundaries;
- a third region located between the functional-circuit blocks and outside of the first and second boundaries, and devoid of functional-circuit blocks;
- a logic circuit disposed in the third region and having an input terminal and an output terminal;
- a first conductive path having a first terminal coupled to the first functional-circuit block and having a second terminal coupled to the input terminal of the logic circuit; and
- a second conductive path having a first terminal coupled to the output terminal of the logic circuit and having a second terminal coupled to the second functional-circuit block.



- functional-circuit blocks spaced apart from one another and each having a respective boundary that surrounds the block;
- a region located between and outside the boundaries of the functional-circuit blocks and devoid of functional-circuit blocks; and
- a repair transistor disposed in the region and having a three terminals, one of the terminals coupled to one of the functional-circuit blocks.
- 22. (currently amended) The integrated circuit of claim 21 wherein two of the transistor terminals are coupled to the <u>one</u> functional-circuit block.
- 23. (currently amended) The integrated circuit of claim 21 wherein the three transistor terminals are coupled to the <u>one</u> functional-circuit block.

24. - 43. (cancelled)

